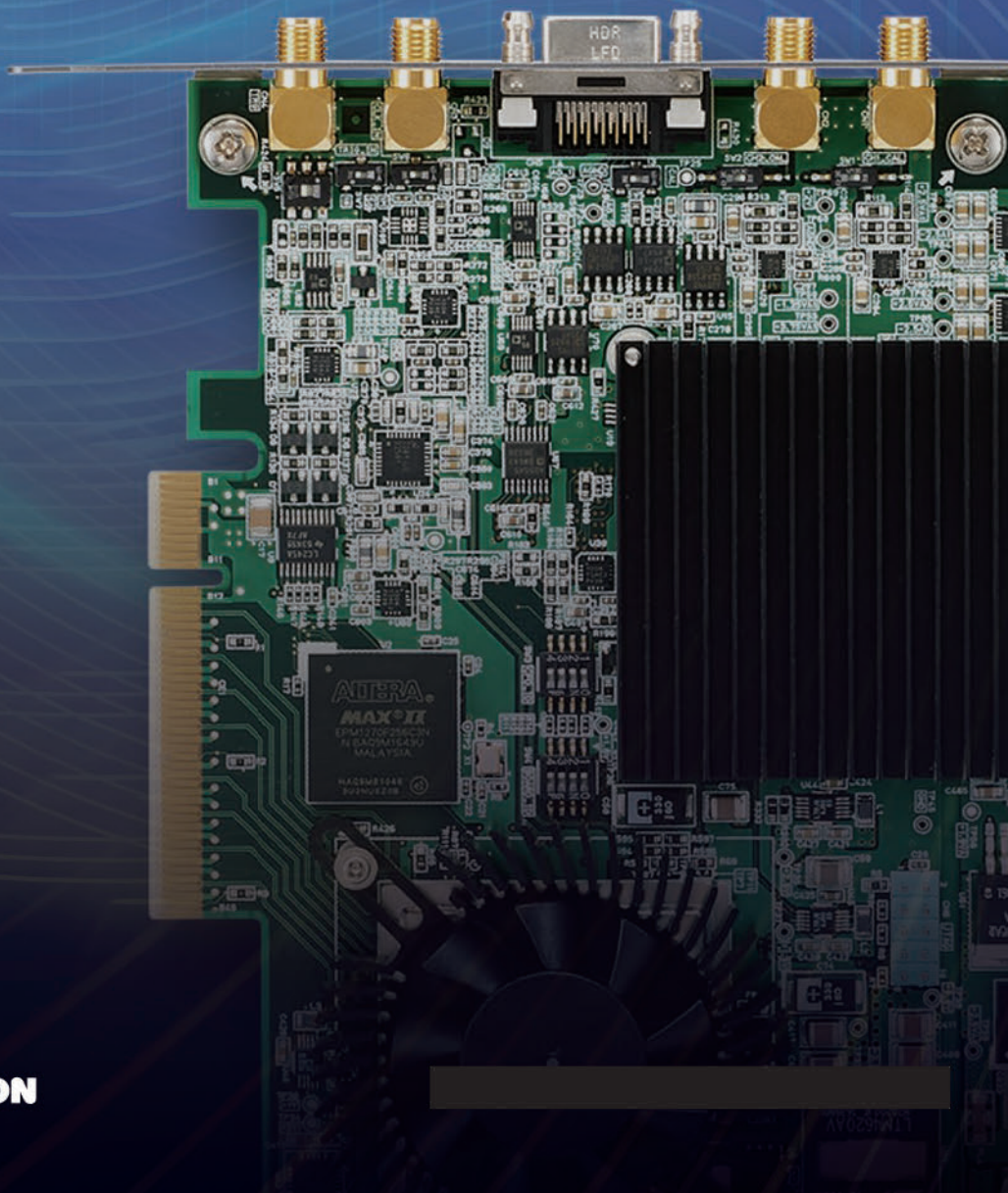
Express Converter

ADC 产品目录

Express Converter

高速数据采集卡系列



AVAL DATA CORPORATION

实现高速 / 高分辨率的自主研发的高速数据采集卡

AVAL DATA的高速模拟板卡 [Express Converter] 系列，是专为满足测量仪器、测试设备及通信设备等领域对高速、高分辨率的需求而开发的产品。

该系列产品结合了高速 ADC 器件与 AVAL DATA自主研发的 PCI Express IP 核技术，实现了采样数据向 PC 的高速传输。

产品支持灵活设定的采样时钟、传输模式与触发设置，可根据用户用途自由调整。
此外，部分产品开放了所搭载的 FPGA 资源，支持用户进行定制开发。

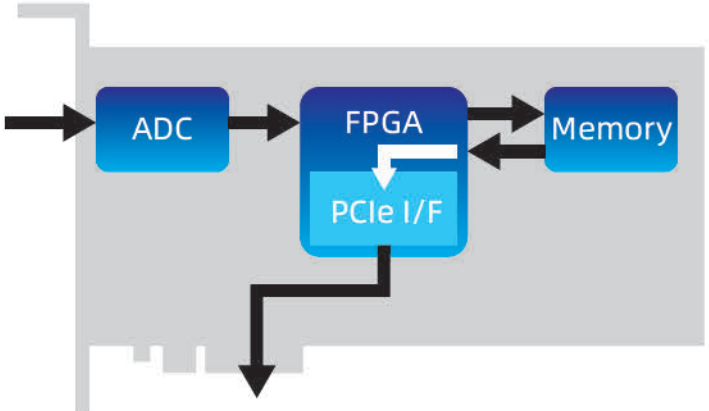
在以海外产品为主导的市场中，作为日本的高速数据采集卡的制造商，我们还提供完善的技术支持与售后服务，致力于为用户带来更加安心的使用体验。

※以下所述的各种功能概要，因机型不同其实现情况和规格也有所差异，详细信息请参阅各产品的使用手册。

采样时钟

各个AD板卡均搭载了PLL器件，可对内部时钟或外部输入时钟进行倍频，以生成所需的采样率，并可使用生成的频率进行采样操作。

内部时钟倍频采样	通过倍频AD板上搭载的内部时钟，生成采样时钟。
外部时钟倍频采样	通过倍频输入的外部时钟，生成采样时钟。
外部时钟直接采样	直接使用输入的外部时钟，作为采样时钟

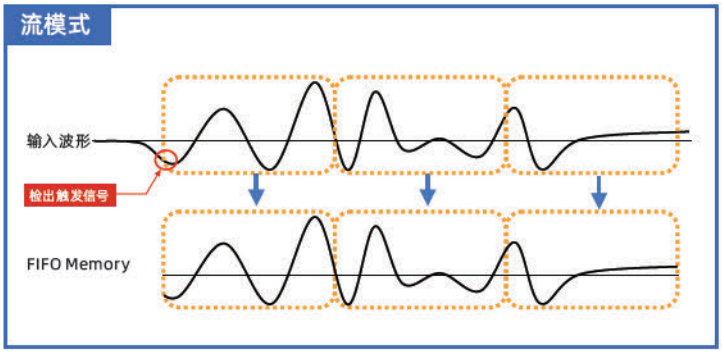


关于高速数据传输模式

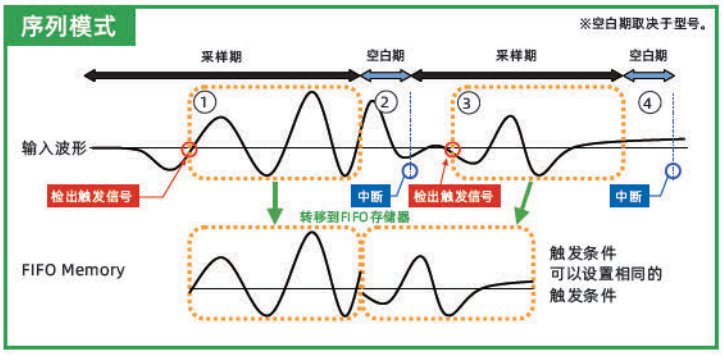
为了实现高速数据传输，配备了两种采样模式：

流模式 (Stream模式)	可连续采集数据的模式。
顺序模式 (Sequence模式)	按触发条件依次执行采样的模式。

流模式

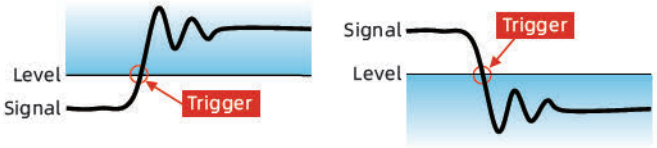
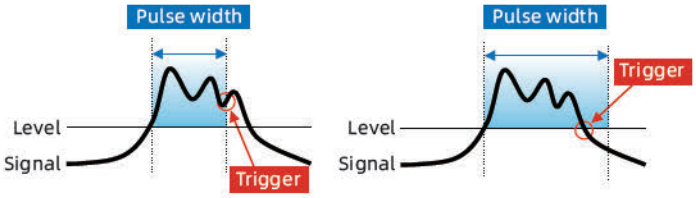


序列模式



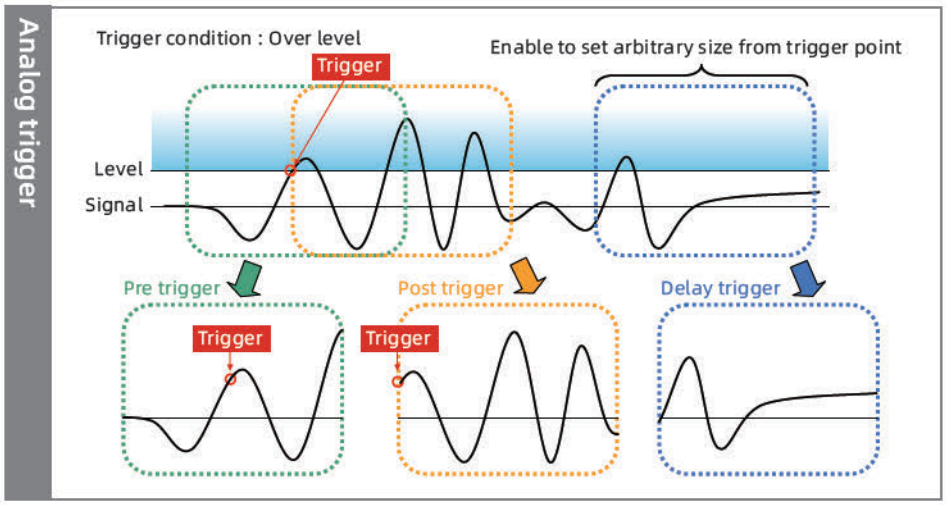
触发功能

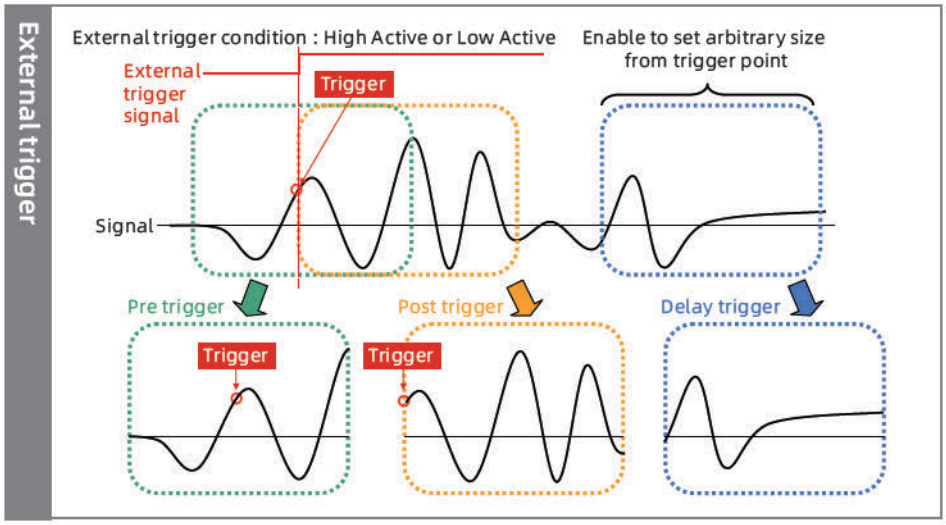
● 各种触发条件

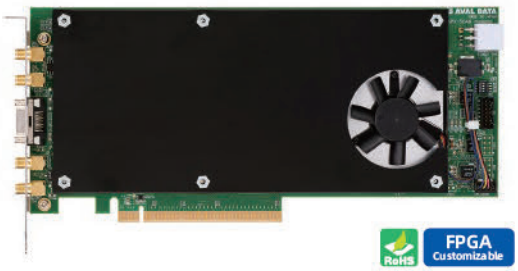
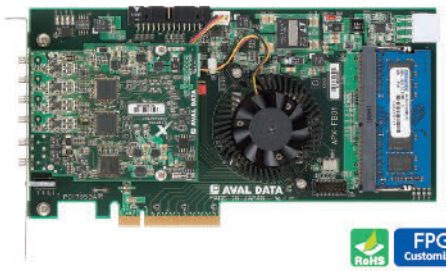
模拟触发	Edge Trigger	以阈值（高于/低于）为条件进行触发 
	Pulse Width Trigger	以某一阈值（上限/下限）和脉冲宽度（小于/大于）为条件进行触发 
外部触发	LVTTL Signal Level Trigger	以活动边缘为条件进行触发
软件触发	—	以活动边缘为条件
可变触发位置 在模拟触发/外部触发条件下可以存储任意大小的数据	Pre Trigger	保存触发条件之前的数据
	Post Trigger	保存触发条件之后的数据
	Delay Trigger	保存触发条件之后的数据（超过触发条件设置的时间）

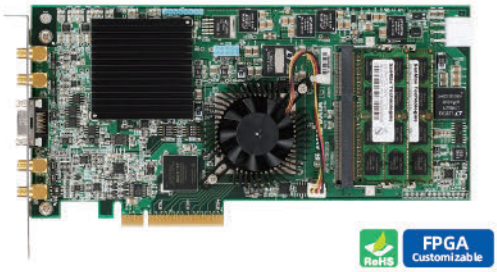
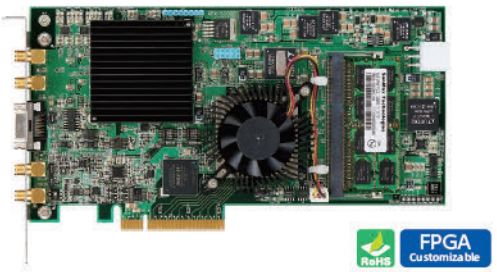
● 可变触发位置

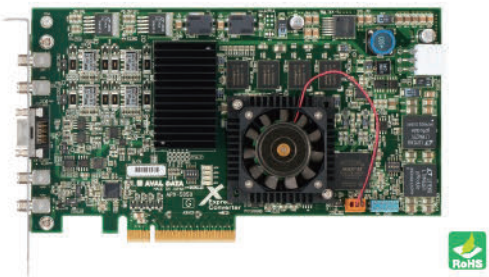
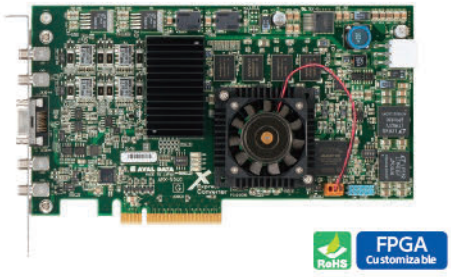
可以任意设置预触发 (Pre Trigger) / 后触发 (Post Trigger) / 延迟触发 (Delay Trigger)





		12bit/3.2GSps/2ch A/D Convert Board **APX-5640**	16bit/500MSps/4ch A/D Convert Board **APX-5056**
			
Model		APX-5640	APX-5056 (APX-FB01+ADF-5056)
Analog I/F	Input	Single end 2 ch (interleaved : single end 1 ch)	Single end 4ch
	Input impedance	50Ω	50Ω
	Coupling	DC Coupling	AC coupling
	Input Range	±0.5V	±1V
	Resolution	12bit	16bit
	Sampling Rate	Max 3.2Gsps(Interleaved 6.4Gsps)	Max.500Msps(2ns)
	Frequency Bandwidth	1.5GHz -3dB(typ.)	250MHz -3dB
	Absolute maxtimum ratings	-	±2V(Current flow) ±1.5V(Non-current flow)
	AC Performance	SFDR: +58~+66dBc(typ.) / SINAD: +53~+55dB(typ.) ENOB: 8.5~8.8bit(typ.) / THD: -65~-61dBc(typ.) SNR: +53~+56dB(typ.)	SFDR: 84.83dBc @10MSps, Fin1MHz SNR : 68.29dBc @10MSps, Fin1MHz ENOB : 11.03bit @10MSps, Fin1MHz
External clock input		Channel : 1 Signal level : 0.6Vp-p~2.0Vp-p Frequency : 10MHz or 100MHz(PLL) Input Impedance : 50Ω(AC coupling) Connector type : SMA	Channel : 1 Signal level : 0.4Vp-p~1.5Vp-p (Sine wave / Square wave) Frequency : 5MHz~100MHz Input Impedance : 1MΩ/50Ω (AC Coupling) Connector type : SMB
External Trigger input		Channel : 1 Signal level : LVTTL Input impedance : 1KΩ/50Ω Connector Type : SMA	Channel : 1 Signal level : LVTTL Input Impedance: 1KΩ/50Ω Connector type : SMB
General Port : DIO		Channel : DI 4ch DO 4ch Signal level : LVTTL Connector Model : HDR-EC26LFDT1-SLD+	Channel : DI 4ch DO 4ch Signal level : LVTTL Connector type : XG4C-2634
Analog Output		Number of output : 2ch Resolution : 16 bit Output Range : -4V~+4V	N/A
Trigger		External Trigger / Analog trigger / Software trigger Analog trigger : Edge, Pulse Trigger position : Pre, Post, Delay	External Trigger / Analog trigger / Software trigger/ Another trigger Analog trigger : Edge, Pulse Trigger Position : Pre, Post, Delay
Maximum Sampling		-	1Gword/1ch
Memory		DDR4 SDRAM Component (8GByte)	DDR4-SDRAM (8Gbyte)
System Bus		PCI Express3.1a (Gen3) 8.0GT/s×16	PCI Express3.0 (Gen3) 8.0GT/s×8
Power		+12V ±8%, 3.4A	+12V±8%, 3.72A
Environment		Temperature 0~50℃, Humidity : 35%~85% (Non condensing)	Temperature : 0~50℃, Humidity : 35%~85% (Non-condensing)
FPGA		XCKU15P-2FFVE1517E (Xilinx)	Kintex UltraScale xcku035-ffva1156-2-e (XILINX)
Dimension (excluding connector)		240.15mm×111.15mm, Panel depth 20mm	205.15mm×106.25mm, Panel depth 20mm
Operating OS		Window10 32bit, 64bit / Window11 64bit	Window10 32bit, 64bit / Window11 64bit
Compliance		RoHS2 (2011/65/EU + (EU) 2015/863)	RoHS
Panel			

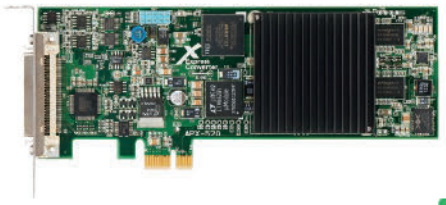
		12bit/1.8GSps/2ch A/D Convert Board **APX-5360G3A**	12bit/1Gbps/2ch A/D Convert Board **APX-5200B-1**
			
Model		APX-5360G3A	APX-5200B-1
Analog I/F	Input	Single end 2ch (Interleaved : Single end 1ch)	Single end 2ch (Interleaved : Single end 1ch)
	Input impedance	50Ω	50Ω
	Coupling	DC Coupling	DC coupling
	Input Range	±0.5V	±0.5V
	Resolution	12bit	12bit
	Sampling Rate	Max 1.8Gsps (Interleaved 3.6Gsps)	Max 1GSps (1ns) / Interleave: 2GSps (0.5ns)
	Frequency Bandwidth	900MHz -3dB (LC Filter Built-in)	900MHz -3dB (LC Filter Built-in)
	Absolute maxtimum ratings	±2V (Current flow) , ±1.5V (Non-current flow)	±2V (current flow) , ±1.5V (Non-current flow)
	AC Performance	SFDR : 68.0dB @1800MSps, Fin1MHz SNR : 56.3dB @1800MSps, Fin1MHz ENOB : 9.0bit @1800MSps, Fin1MHz	SFDR : 72.18dBFs @1000MSps, Fin1MHz SNR : 59.41dBFs @1000MSps, Fin1MHz ENOB : 9.53bit @1000MSps, Fin1MHz
External clock input		Channel : 1 Signal level : 0.4Vp-p ~1.5Vp-p (Sine wave / Square wave) Frequency : 5MHz~100MHz(PLL) 150MHz~1800MHz (Direct Sampling) Input Impedance : 1MΩ/50Ω (AC coupling) Connector type : SMA	Channel : 1 Signal level : 0.4Vp-p ~1.5Vp-p (Sine wave / Square wave) Frequency : 5MHz~100MHz (PLL) 150MHz~1000MHz (Direct Sampling) Input impedance : 1MΩ / 50Ω (AC Coupling) Connector Type : SMA
External Trigger input		Channel : 1 Signal level : LVTTL Input impedance : 1KΩ/50Ω Connector Type : SMA	Channel : 1 Signal level : LVTTL Input impedance : 1KΩ/50Ω Connector Type : SMA
General Port : DIO		Channel : DI 4ch DO 4ch Signal level : LVTTL Connector Model : HDR-EC26LFDT1-SLD+	Channel : DI 4ch DO 4ch Signal level : LVTTL Connector Model : HDR-EC26LFDT1-SLD+
Analog Output		Number of output : 2ch Resolution : 16 bit Output Range : -4V~+4V	Number of output : 2ch Resolution : 16 bit Output Range : -4V~+4V
Trigger		External Trigger / Analog trigger / Software trigger Analog trigger : Edge, Pulse Trigger position : Pre, Post, Delay	External Trigger / Analog trigger / Software trigger Analog trigger : Edge, Pulse Trigger position : Pre, Post, Delay
Maximum Sampling		2G word / 2ch,4G word /1ch	2G word / 2ch, 4G word / 1ch
Memory		DDR3-SDRAM(8Gbyte)x2	DDR3-SDRAM (8G Byte)
System Bus		PCI Express3.0 (Gen3) 8.0GT/s×8	PCI Express2.0 (Gen2) 5.0GT/s×8
Power		+12V ±8%, 3.4A	+12V±8%, 3.3A
Environment		Temperature : 0~50℃, Humidity : 35%~85% (Non-condensing)	Temperature 0~50℃, Humidity : 35%~85% (Non condensing)
FPGA		5GXMA3K1F40I2N (Intel)	5SGXMA3K1F40C2N (Intel)
Dimension (excluding connector)		220.15mm×106.65mm, Panel depth 20mm	212.5mm×111.15mm, Panel depth 20mm
Operating OS		Window10 32bit, 64bit / Window11 64bit / Linux	Window10 32bit, 64bit / Window11 64bit / Linux
Compliance		RoHS	RoHS
Panel			

		12bit/500MSps/2ch A/D Convert Board **APX-5050** ※	14bit/400MSps/2ch A/D Convert Board **APX-5040**
			
Model		APX-5050	APX-5040
Analog I/F	Input	Single end 2ch	Single end 2ch
	Input impedance	50Ω	50Ω
	Coupling	DC coupling	DC coupling
	Input Range	±2V, ±1V, ±500mV	±2V, ±1V, ±500mV
	Resolution	12bit	14bit
	Sampling Rate	Max. 500MSps(2.5ns)	Max. 400MSps(2.5ns)
	Frequency Bandwidth	200MHz -3dB (LC filter built-in)	200MHz -3dB (LC filter built-in)
	Absolute maxtimum ratings	±5V (Current flow) ±2V (Non-current flow)	±5V (Current flow) ±2V (Non-current flow)
	AC Performance	SFDR : 68.54dBFs @500MSps, Fin10MHz SNR : 57.33dBFs @500MSps, Fin10MHz ENOB : 9.23bit @500MSps, Fin10MHz	SFDR : 80.73dBFs @400MSps, Fin1MHz SNR : 60.56dBFs @400MSps, Fin1MHz ENOB : 9.75bit @400MSps, Fin1MHz
External clock input		Channel : 1 Signal level : 0.7Vp-p(typ)(Sine wave/ Square wave) Frequency : 5MHz~100MHz (PPL) 40MHz~500MHz (Direct sampling) Input Impedance : 1MΩ/50Ω (AC Coupling) Connector type : SMA	Channel : 1 Signal level : 0.7Vp-p(typ)(Sine wave/ Square wave) Frequency : 5MHz~100MHz (PPL) 20MHz~400MHz (Direct sampling) Input Impedance : 1MΩ/50Ω (AC Coupling) Connector type : SMA
External Trigger input		Channel : 1 Signal level : LVTTL (5V Tolerant) Input impedance : 1KΩ/50Ω Connector type : SMA	Channel : 1 Signal level : LVTTL (5V Tolerant) Input impedance : 1KΩ/50Ω Connector type : SMA
General Port : DIO		Channel : DI 4ch DO 4ch Signal level : LVTTL Connector Model : HDR-EC26LFDT1-SLD+	Channel : DI 4ch DO 4ch Signal level : LVTTL Connector Model : HDR-EC26LFDT1-SLD+
Analog Output		Channel : 2ch Resolution : 16bit Output range : -4V~+4V	Channel : 2ch Resolution : 16bit Output range : -4V~+4V
Trigger		External Trigger / Analog trigger / Software trigger Analog trigger : Edge, Pulse Trigger Position : Pre, Post, Delay	External Trigger / Analog trigger / Software trigger Analog trigger : Edge, Pulse Trigger Position : Pre, Post, Delay
Maximum Sampling		256M word / 1ch	256M word / 1ch
Memory		DDR3-SDRAM (2Gbyte)	DDR3-SDRAM (2Gbyte)
System Bus		PCI Express2.0 (Gen2) 5.0GT/s×8	PCI Express2.0 (Gen2) 5.0GT/s×8
Power		+12V±9%, 3.75A	+12V±8%, 3.75A
Environment		Temperature : 0~50℃, Humidity : 35%~85% (Non-condensing)	Temperature : 0~50℃, Humidity : 35%~85% (Non-condensing)
FPGA		EP4SGX180HF35C2N (Intel)	EP4SGX180HF35C2N (Intel)
Dimension (excluding connector)		192.65mm×111.15mm, Panel depth 20mm	192.65mm×111.15mm, Panel depth 20mm
Operating OS		Window10 32bit, 64bit / Window11 64bit / Linux	Window10 32bit, 64bit / Window11 64bit / Linux
Compliance		RoHS	RoHS
Panel			

※When sampling at 500 MHz, it may be issued by Glitch which causes a bit error in ADC.

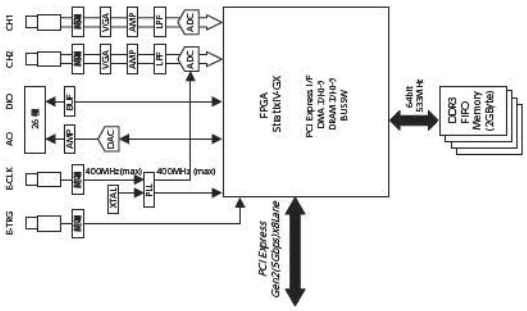
18bit/200KHz/16ch A/D Convert Board

APX-520

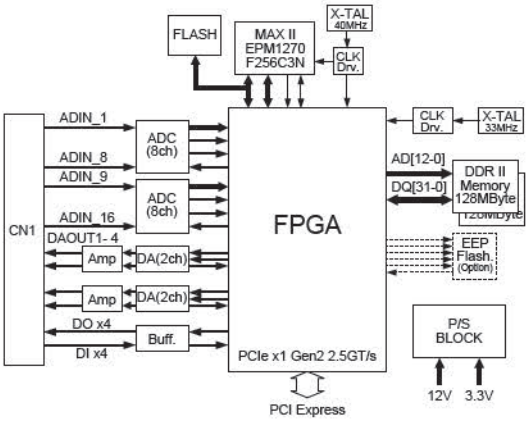


Model			APX-520
Analog I/F	Input (Simultaneous sampling)		16
	Sampling clock		MAX 200KHz
	Resolution		18bit
	Anti-aliasing filter		22KHz@-3dB(±10V)/15KHz@-3dB(±5V)
	Input impedance		1MΩ
	Input current		5.4μA @+10V
	Coupling		DC Fixed
	Input Range	1MΩ	±5V or ±10V
	Absolute maxtimum ratings	1MΩ	±16.5V
Analog Output	Output		4ch
	Resolution		16bit
	Output range		-5V~+5V
DIO	Input	Number	4ch
		Signal level	LVTTL (5V Tolerant)
	Output	Number	4ch
		Signal level	LVTTL (+3.3V Output)
Trigger/ Clock	Internal clock		1Hz to 200KHz in 1Hz increments (*Adjusted to the available configurable clocks)
	External Trigger		Input is possible from DI in units of AD8ch
Host I/F			PCI Express2.0 (Gen2) 2.5GT/s×1
Power			+3.3V±9% 280mA +12V±8% 510mA
Environment			Temperature : 0~50℃, Humidity : 35%~85% (Non-condensing)
Dimension (excluding connector)			120mm×64mm, Panel depth 20mm
Operating OS			Window10 32bit, 64bit / Window11 64bit
Compliance			RoHS
Panel			

APX-5040 Block diagram



APX-520 Block diagram



High-speed AD 160Msps 4CH
High-speed analog signal processing unit

ALG-160M04-L2

Ideal for environmental LIDAR measurement Signal processing unit

Features

◎ Up to 160MHz High speed AD conversion

◎ Up to 40MHz High speed DI

◎ FPGA High-speed signal processing

◎ With general-purpose I/F LAN, Easy host connection

◎ SDK for unit control

◎ Signal processing specialized for H13126-01/02 manufactured by Hamamatsu Photonics Co., Ltd.

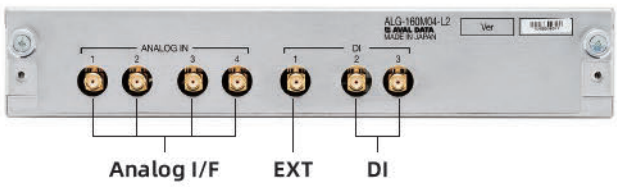
◎ Included software allows synthesis processing of analog and digital signals.
*No need for host signal processing

Main Specifications

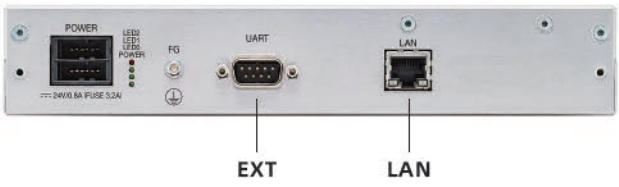
Model name		ALG-160M-04
Analog I/F		1~160Msps / 4ch / 14bit
CPU		ARM CortexA53(2Core) CortexR5(2Core)
Storage / Memory		SSD 128G / DDR3 8G
Power supply		DC12V(24V)
Digital Input		MAX : 40MHz/2ch
External trigger I/F		MAX : 10MHz /1ch
I/F		LAN(GbE) x1ch / EtherCAT x1ch USB3.0 x1ch / DIO
Log time (SSD) ※	Raw	80sec / 4ch (160Msps)
	10averaging	800sec / 4ch (160Msps)

※Logging time varies depending on sampling conditions and other factors.

Front



Back

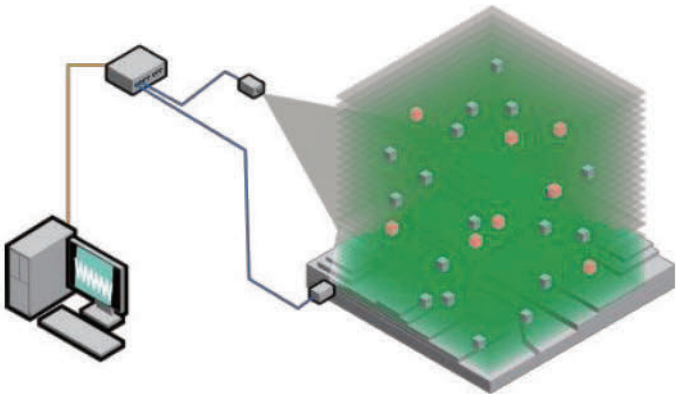


Data processing suitable for environmental Lidar measurement

◎ Synchronize with the laser excitation trigger to respond to up to 100,000 lineintegration processes.

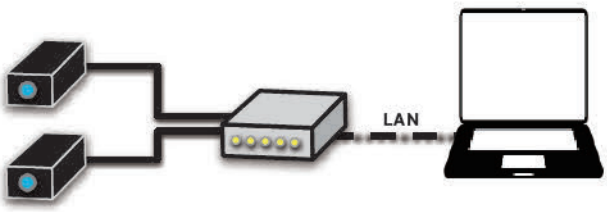
◎ Measure 1 to 2 H13126-01/02 simultaneously

◎ Up to 10 (H13126-01/02:20) connections to your PC via Ethernet.

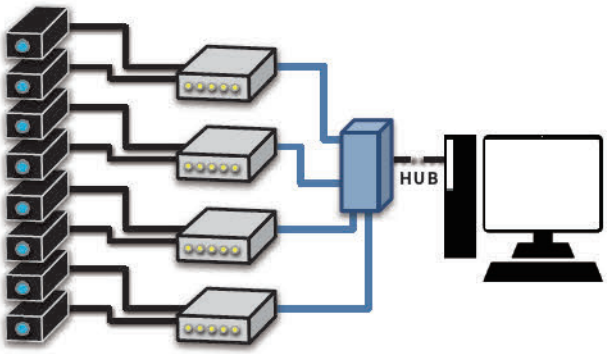


Example of use

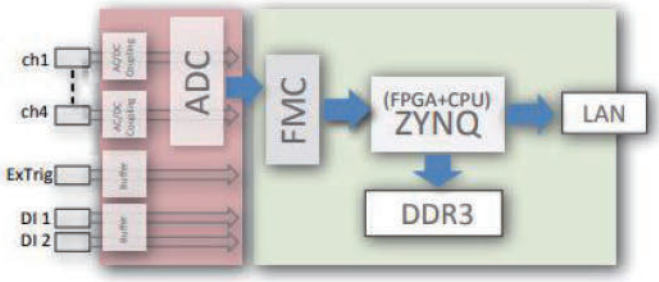
1) Connect 2 units of Hamamatsu Photonics H3126-01/02



2) HUB by ALG-160M04-L2 Connect multiple units



Block Diagram



Manufactured by Hamamatsu Photonics
Wide dynamic range
Photomultiplier tube module
H13126-01/02

FPGA Customization

FPGA Customization of the APX-5040 : FDK-APX5040

FDK-APX5040是用于APX-5040的FPGA信号处理的FPGA开发套件。提供了" FPGA项目"、"样品源码"、"各种文档"、"寄存器访问工具"作为开发环境，以在FPGA上添加您的信号处理功能。

■ FDK-APX5040 Package Configuration

- ◆ Tool/Sample : 寄存器访问，示例代码
  (FFT Sample code processable from 1024/4096)
- ◆ Projector : 示例设计 (s000)
- ◆ Document : 设计顺序、注意事项等。

■ Development Environment

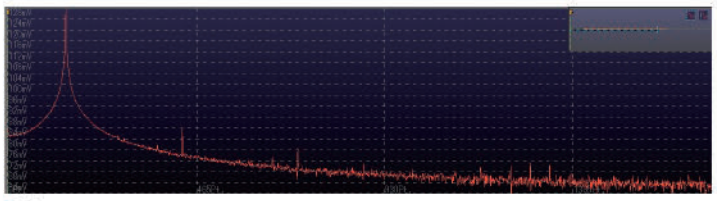
- ◆ Quartus II Ver.12.2 SP1 (与订阅版兼容)
  ※ 不支持Web版
- ◆ 需要许可证以编译加密的源代码
- ◆ 不支持从主机到APX-5040的DMA。
- ◆ 需要USB-Blaster (APX-5040未附带)

■ FPGA Development Programming

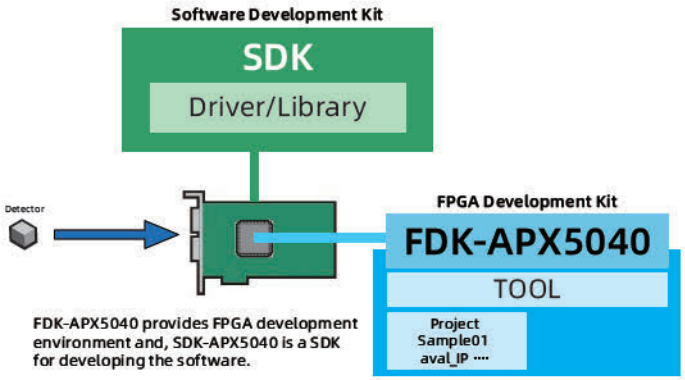
FDK-APX5040提供了Quartus开发环境的各种文件 (FPGA处理开发流程: 第■部分) 用户设计和Avaldata设计的源代码 (Aval IP /触发逻辑) 经过成后成为输入文件 (pof文件)。

Development Example

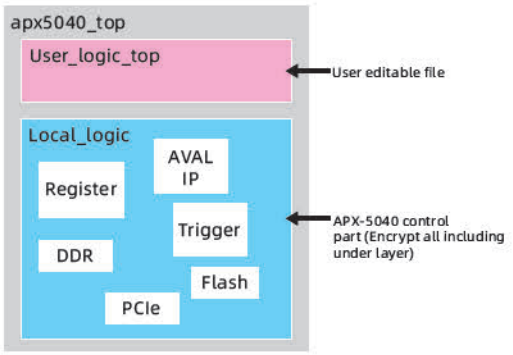
以下是使用DMA通过在用户逻辑中计算功率谱来传输数据的示例的图表。



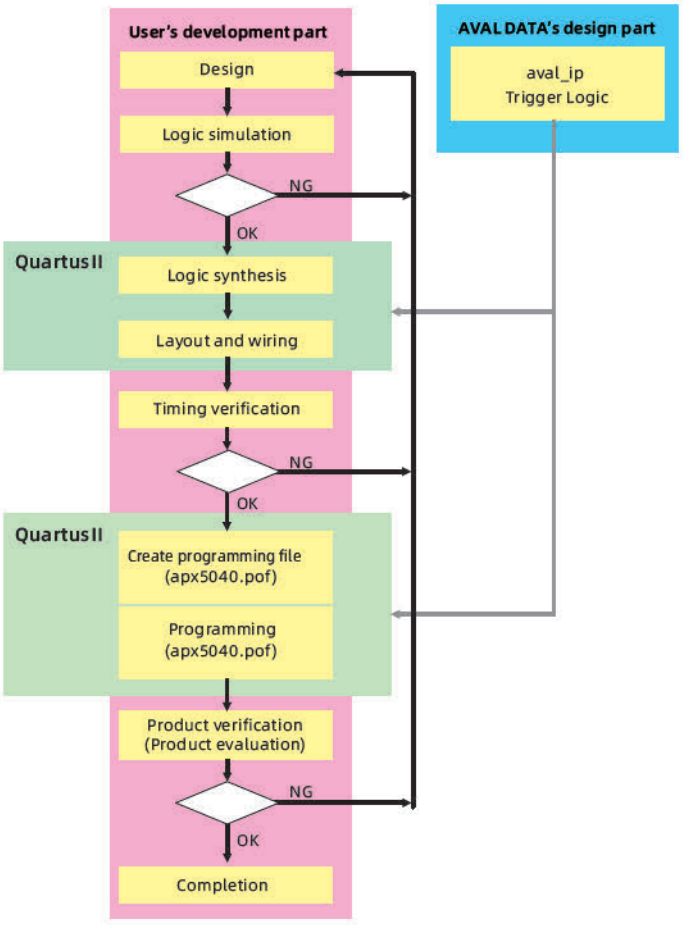
Development of FPGA Processing and Capture Software



FPGA Design Configuration

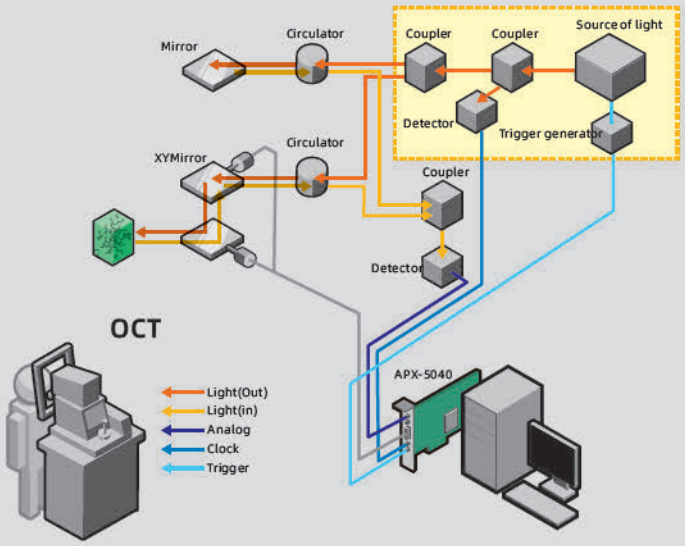


FPGA Processing Development Flow

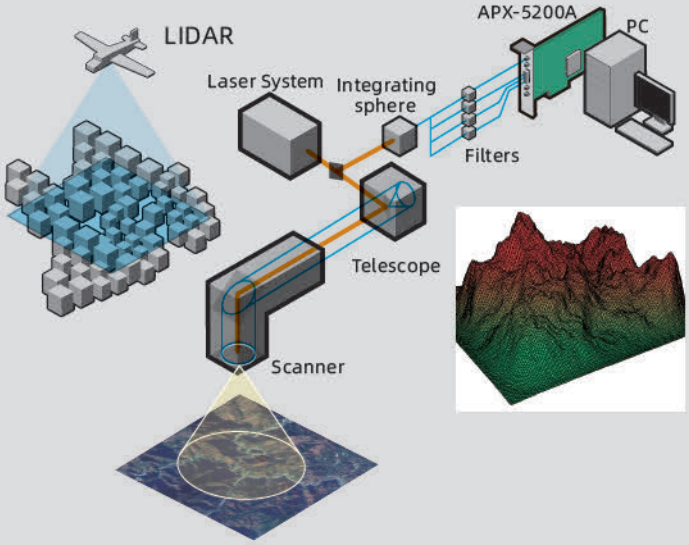


Applications

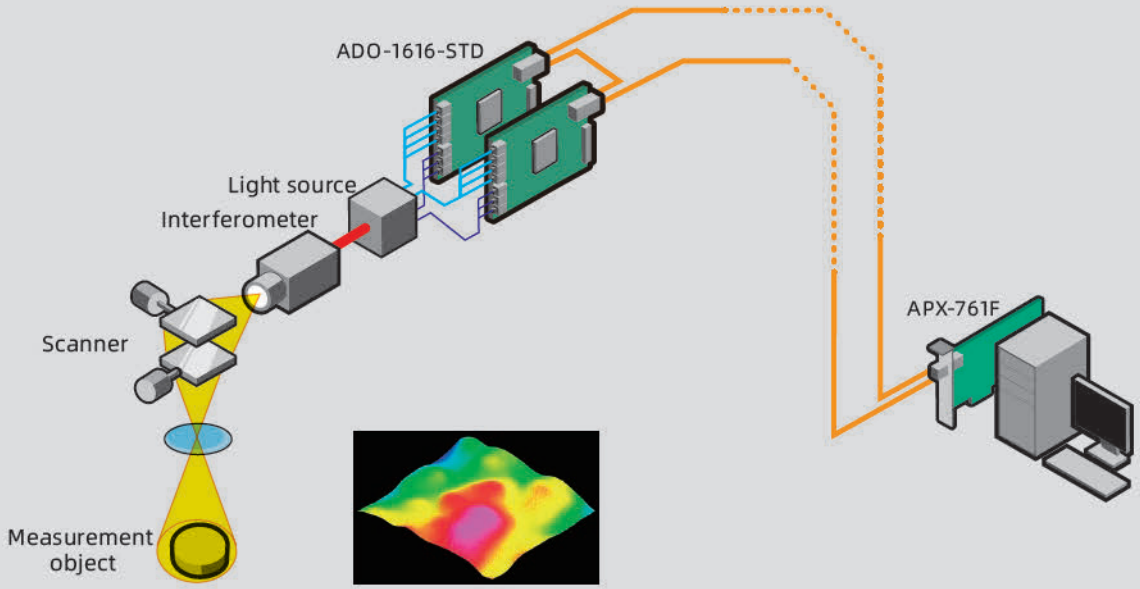
医疗设备



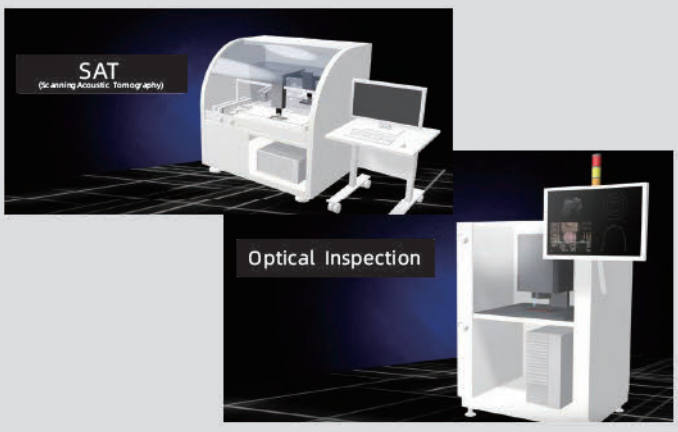
检测设备



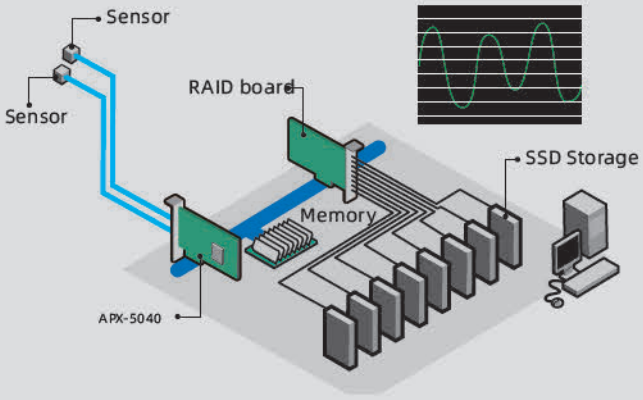
3D检测设备



工业用 OCT



大数据log系统



Software

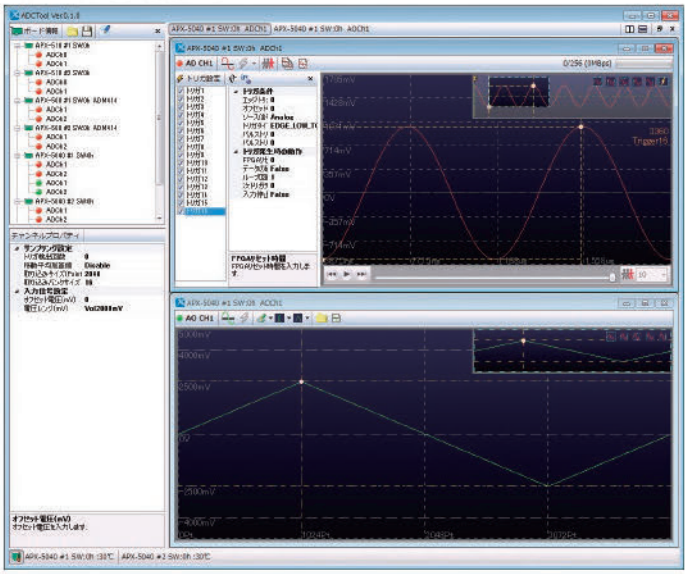
Software Development

AVAL DATA准备了适用于Windows和Linux的驱动程序库。同时还提供了现成的评估工具，可以执行板卡控制、波形显示、AIP日志、性能显示和连续存储。

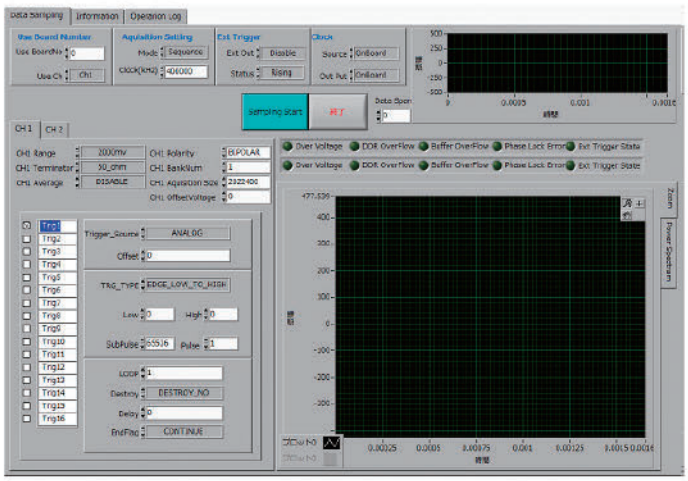
■ **Windows.Net评估工具 (AWP-ADCTOOL-01)** 该工具用于在购买后进行评估，以评估和控制硬件在开发应用程序之前的性能。

■ **LabVIEW VI示例(AWP-ADCLV-01)** 该示例用于从LabVIEW操作硬件。通过将其设置为每个功能 (每个SDK的API) 的VI，可以在LabVIEW上进行详细操作。

AWP-ADCTOOL-01



AWP-ADCLV-01



AVAL GLOBAL Co.,Ltd

C-607, 338 Gwanggyojungang-ro, Suji-gu, Yongin-si, Gyeonggi-do, South Korea 16942

TEL +82-70-7019-1420 E-MAIL sales@aval-global.com URL www.aval-global.com

As of Apr. 2025